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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,123	07/30/2003	Wenkwei Lou	BP2621	6723
34399	7590	11/01/2007	EXAMINER	
GARLICK HARRISON & MARKISON			LAMARRE, GUY J	
P.O. BOX 160727			ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/630,123	LOU, WENKWEI
	Examiner	Art Unit
	Guy J. Lamarre	2112

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 17 October 2007.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-22 is/are pending in the application.
 4a) Of the above claim(s) 5-8 and 12-22 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-4 and 9-12 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 30 July 2003 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____.
 4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

DETAILED ACTION

* Pursuant to restriction requirements, **Claims 5-8 and 13-22** are withdrawn and cancelled; **Claims 1-4, 9-12** remain pending.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-4, 9-12 are rejected under 35 U.S.C. 102(e) as being anticipated by (USP. No. 6535146; filed June 15, 2000) to **Chang et al.**

As per **Claims 1-4, 9-12, Chang et al.** discloses equivalent detection of short-circuits/errors in keyboard Matrix/user input device comprising switch matrix (col. 1 line 22 et seq.); scan logic (e.g., col. 1 line 30 et seq., col. 2 line 5) operable to detect signals corresponding to operation of said rows and columns of said switch matrix and to generate an output signal in response thereto; a test control bus (e.g., col. 2 lines 36 et seq.) operable to provide test signals to said scan logic; a storage module (e.g., col. 2 lines 11, 33 et seq.) for storing an executable test sequence program for generating a plurality of signals corresponding to a known operating condition of said switch matrix; a general purpose input-output (GPIO) module/unit operable to provide said a plurality of test signals to said scan logic via said test control bus; and a processor operable to initiate execution of said executable test sequence program and further operable to compare said output signal of said scan logic to a known reference signal to obtain an indication of the operating condition of said scan logic, in, e.g., Fig. 4: block 11-22 and col. 2 lines 45, 57 et seq.

'a method of detecting short-circuits of a keyboard, which can be built into a computer system installed with a keyboard, allowing a tester to detect and determine short-circuit of the keyboard...

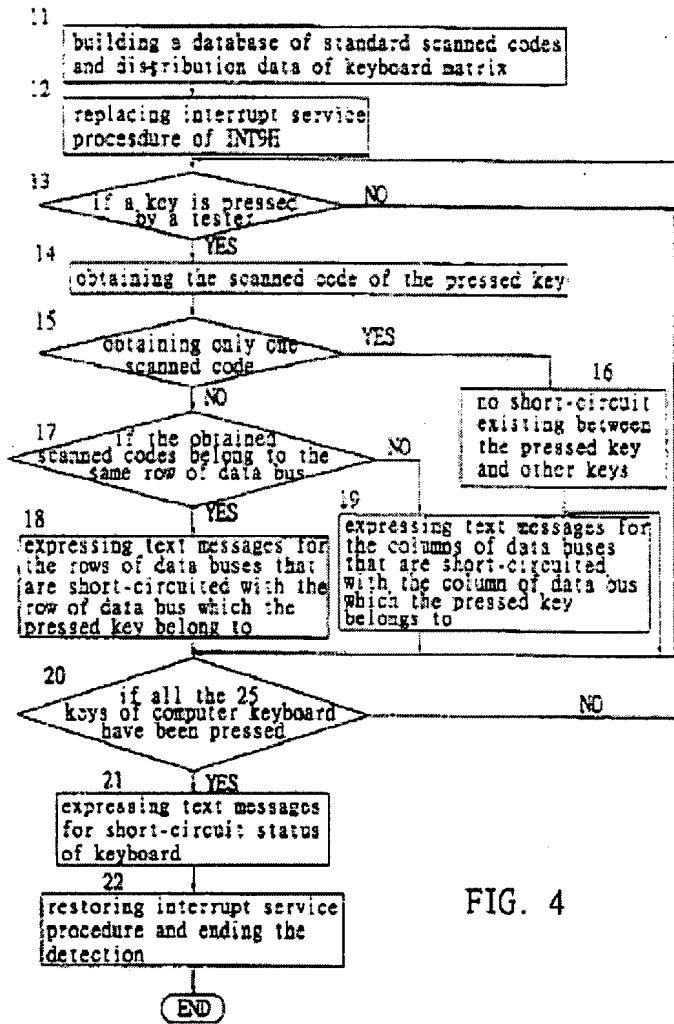


FIG. 4

As per Claims 1, 9, Chang et al. discloses equivalent detection of short-circuits/errors in keyboard Matrix/user input device comprising switch matrix (col. 1 line 22 et seq.); scan logic (e.g., col. 1 line 30 et seq., col. 2 line 5) operable to detect signals corresponding to operation of said rows and columns of said switch matrix and to generate an output signal in response thereto; a test control bus (e.g., col. 2 lines 36 et seq.) operable to provide test signals

to said scan logic; a storage module (e.g., col. 2 lines 11, 33 et seq.) for storing an executable test sequence program for generating a plurality of signals corresponding to a known operating condition of said switch matrix; a general purpose input-output (GPIO) module/unit (e.g., col. 2 line 35 et seq.) operable to provide said a plurality of test signals to said scan logic via said test control bus; and a processor operable to initiate execution of said executable test sequence program and further operable to compare said output signal of said scan logic to a known reference signal to obtain an indication of the operating condition of said scan logic, in, e.g., Fig. 4:*block 11-22* and col. 2 lines 45, 57 et seq.

As per Claims 2, 10, Chang et al. discloses equivalent user input device of claim 1, wherein the test signals provided by the GPIO module comprise a minidriver e.g., in col. 2 line 35 et seq.

As per Claims 3, 11, Chang et al. discloses equivalent user input device of claim 1, wherein the scan logic operates in first and second states (e.g., col. 2 lines 35, 45 et seq.), wherein said scan logic receives signals from said switch matrix in said first state and wherein said scan logic receives test signals from the test control bus in said second state, e.g., in col. 1 line 65 et seq.

As per Claims 4, 12, Chang et al. discloses equivalent user input device of claim 3, wherein the GPIO module (e.g., col. 2 lines 35, 45 et seq.), is operable to switch said scan logic from said first state to said second state in response to control signals generated by said processor, e.g., in col. 1 line 65 et seq.

Claim Objections

2. It is unclear to the Examiner what is meant by '*a switch matrix having a plurality of plurality of rows and columns.*' Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the **second** paragraph of 35 U.S.C. 112:

.The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

.1 **Claims 2, 10** are rejected under the second paragraph of 35 U.S.C. 112. It is unclear to the Examiner what is meant by '*test signals ... comprise minidriver*'.

Abstract

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

.1 The abstract of the disclosure is objected to because said abstract exceeds 150 words..

Appropriate correction is required.

CONCLUSION

* Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (571) 273-8300 for all formal communications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (571) 272-3826. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached at (571) 272-6962.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-3609.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Guy J. Lamarre, P.E
Primary Examiner
